IN THE CLAIMS

Please amend the claims as follows:

Claims 1-27 (Canceled).

Claim 28 (Currently Amended): A semiconductor memory device comprising:

a semiconductor element;

a plurality of lead wires connected to a plurality of connecting electrodes formed on said semiconductor element;

at least a single dummy lead wire that is not electrically connected to said semiconductor element and does not include an outer lead portion for electrically connecting said semiconductor element to an external circuit of said semiconductor element;

an insulating film having an opening portion configured to accommodate said semiconductor element and to support said plurality of lead wires connected to the plurality of connecting electrodes of the semiconductor element and said at least the single dummy lead wire, said opening portion having a plurality of sides that define a perimeter of said opening portion; and

a resin molding configured to cover a connecting portion between tip portions of the plurality of lead wires and the plurality of connecting electrodes and a tip portion of said at least the single dummy lead wire within the opening portion of said insulating film,

wherein said at least a single dummy lead wire is arranged in a space defined by two adjacent lead wires of said plurality of lead wires so that a length of said space is at least twice a minimum pitch between adjacent lead wires of said plurality of lead wires, the two adjacent lead wires being provided on one side of said plurality of sides of the insulating film to define the space on the one side of the insulating film.

Claim 29 (Currently Amended): A semiconductor memory device comprising:

a semiconductor element;

a plurality of lead wires connected to a plurality of connecting electrodes formed on said semiconductor element;

at least a pair of dummy lead wires that are not electrically connected to said semiconductor element and do not include an outer lead portion for electrically connecting said semiconductor element to an external circuit of said semiconductor element;

an insulating film having an opening portion configured to accommodate said semiconductor element and to support said plurality of lead wires connected to the plurality of connecting electrodes of the semiconductor element and said at least the pair of dummy lead wires, said opening portion having a plurality of sides that define a perimeter of said opening portion; and

a resin molding configured to cover a connecting portion between tip portions of the plurality of lead wires and the plurality of connecting electrodes and a tip portion of said at least the pair of dummy lead wires within the opening of said insulating film,

wherein one and the other of said at least the pair of dummy lead wires are provided on one side and an opposite side of said plurality of sides of said insulating film, respectively, each of the one and the other of said at least the pair of dummy lead wires being arranged in corresponding first and second spaces defined by first and second two adjacent lead wires of said plurality of lead wires, respectively, so that a length of each said first and second spaces is at least twice a minimum pitch between adjacent lead wires of said plurality of lead wires, said first two adjacent lead wires being provided on said one side of said insulating film to define said first space on said one side of said insulating film, and said second two adjacent lead wires being provided on said opposite side of said insulating film to define said second space on said opposite side of said insulating film.

Claim 30 (New): A semiconductor memory device according to claim 28, wherein a semiconductor chip in which the semiconductor element is formed has a thickness of approximately 50 μm.

Claim 31 (New): A semiconductor memory device according to claim 29, wherein a semiconductor chip in which the semiconductor element is formed has a thickness of approximately 50 μm.

Claim 32 (New): A semiconductor memory device according to claim 28, wherein a tip portion of the at least a single dummy wire does not extend over the semiconductor element.

Claim 33 (New): A semiconductor memory device according to claim 29, wherein tip portions of the at least a pair of dummy wires do not extend over the semiconductor element.

Claim 34 (New): A semiconductor memory device according to claim 28, wherein a tip portion of the at least a single dummy wire extends over the semiconductor element.

Claim 35 (New): A semiconductor memory device according to claim 29, wherein tip portions of the at least a pair of dummy wires extend over the semiconductor element.

Claim 36 (New): A semiconductor memory device according to claim 28, wherein tip portions of at least two dummy wires extend over the semiconductor element and the tip portions of the at least two dummy wires are connected to each other on the semiconductor element.

Claim 37 (New): A semiconductor memory device according to claim 29, wherein tip portions of the at least a pair of dummy wires extend over the semiconductor element and the tip portions of the at least a pair of dummy wires are connected to each other over the semiconductor element.